

Siddharth Patel

Undergraduate Researcher · Electrical & Computer Engineering · Shiv Nadar Institution of Eminence

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Research interests: hardware for AI and computer architecture; memory systems and compute-in-memory; digital VLSI and SoC design; efficient and adaptive AI inference.

EDUCATION

Shiv Nadar Institution of Eminence, Greater Noida, India

Aug 2023 – May 2027 (expected)

B.Tech in Electrical & Computer Engineering, specialization in Nanoelectronics & Embedded Systems

- **CGPA 8.75/10** (top 10%) · **Dean's List: Fall 2023, Spring 2024, Fall 2025, Spring 2026**
- **Student of the Year, Class of 2027**, sole university-wide recipient across all departments (2026)
- Thesis: *An Open-Source GPU Microarchitecture: A Patent-Unencumbered Design with Synthesizable RTL* (in progress; advisor: Dr. Rohit Singh)
- Selected coursework: Computer Organization & Design, ASIC: RTL-to-GDS, VLSI Design, Digital Design with FPGAs, Semiconductor Devices, Embedded Systems, Deep Learning, Large Language Models

PUBLICATIONS

[†] corresponding author · my name in bold

Peer-reviewed conference papers

- [1] **S. Patel[†]** and R. Singh. "Hardware-Enabled Root of Trust for IoT Security." In *Proc. IEEE International Conference on Intelligent Systems and Embedded Design (ISED)*, 2025. DOI
- [2] S. V. Rajeshwaran, O. Singh, **S. Patel**, S. Singhal, and R. Singh. "Design and Implementation of a Smart Power Controller for Sensor Nodes." In *Proc. International Conference on Intelligent Technologies for a Sustainable & Inclusive Future (ICITSIF)*, 2026. DOI

Under review

- [3] **S. Patel[†]**, A. Awasthi, A. Chaurasia, and R. Singh. "Bitwise-Reproducible Reduction Across Cluster Reshape: A Compiler/Fabric ABI." *IEEE Transactions on Parallel and Distributed Systems*, 2026. Code
- [4] **S. Patel[†]** and R. Singh. "AI Hardware Accelerators for Large Language Models: Architectures and the Memory Wall." *ACM Computing Surveys*, 2026. [arXiv:2608.28048](https://arxiv.org/abs/2608.28048)
- [5] **S. Patel** and R. Singh. "RMAI: Runtime Multi-Objective Adaptive Inference through Joint Dynamic Sparsity and Precision Scaling on Resource-Constrained IoT Edge Devices." *IEEE Internet of Things Journal*, 2026.
- [6] **S. Patel[†]**, V. Singh, S. Malu, and R. Singh. "Learn the Interface, Not the Implementation: Output Representation Dominates Training Regime in LLM-Based RTL Generation." *40th IEEE International Conference on VLSI Design (VLSID)*, 2027.

RESEARCH EXPERIENCE

GPU Microarchitecture from First Principles (Undergraduate Thesis)

2026 – Present

Advisor: Dr. Rohit Singh

- Defining a custom GPU ISA and microarchitecture that targets synthesizable SystemVerilog RTL on a Nexys A7 (Artix-7) FPGA, to be released as open source for research and teaching.
- Built a basic C++ instruction-set simulator as the golden reference model; single-core RTL co-simulated against it is the next milestone.

Deterministic Large-Model Inference on Parallel Hardware

Dec 2025 – Present

Advisors: Dr. Rakesh Palishtty and Dr. Rohit Singh

- Designed a compiler/fabric ABI that makes 64-bit floating-point reductions bit-identical across changes in worker count, topology and schedule; co-designed the parameterized NoC fabric (3.7k lines of SystemVerilog) [3].
- Validated 2,822 compiler-generated configurations in cycle-accurate RTL simulation with zero bit divergence; the checking oracle caught 84/84 injected faults.
- Found a performance-counter methodology error that had corrupted 54% of cycle counts (140 fell below a proven lower bound) and fixed the measurement pipeline.

RMAI: Runtime Adaptive Inference for Edge Devices

Oct 2025 – May 2026

Advisor: Dr. Rohit Singh

- Designed a runtime framework that jointly tunes per-layer weight sparsity and quantization precision to live device state (battery, thermal, memory) [5].
- Up to 14.8% lower latency and 15.4% energy savings over a static INT8 baseline on ResNet-50 (Raspberry Pi 4); validated on ResNet-50, MobileNetV2, DeiT-Small and YOLOv8m.

Smart Power Controller for Sensor Nodes

Dec 2024 – Oct 2025

Research Assistant · Advisor: Dr. Rohit Singh

- Contributed to an energy-efficient wireless sensor node with a programmable power-control unit for smart-irrigation and smart-city use; demand-based power management doubled battery life [2].

Hardware Root of Trust for IoT Security

Aug 2023 – Dec 2024

Advisor: Dr. Rohit Singh

- Designed a hardware root of trust with immutable device identities and RSA-OAEP secure boot to resist spoofing and tampering; 99.8% authentication accuracy under simulated attacks [1].

INDUSTRY EXPERIENCE

STMicroelectronics

Jun 2026 – Aug 2026

Technology R&D Intern · Greater Noida, India

- Automated ECC memory design: replaced a manual, multi-engineer, per-variant RTL flow with a Python generator producing synthesis-ready SEC/SECDED encoder/decoder RTL across 7+ configuration axes.
- Studied LLM-based RTL generation across 4 output representations and 7 training regimes; a ~10M-parameter from-scratch model reached 0.887 formal equivalence at $\sim 1,600\times$ less energy per correct design than a 32B fine-tune [6].
- Built a 6-stage verification harness (exhaustive fault injection, formal equivalence, synthesis) and a spec-driven UVM testbench for an APB slave that found and fixed 4 RTL bugs.

Independent Consultant, Electronics Design

Feb 2025 – Jul 2025

Electronics manufacturer · Delhi NCR, India

- Sole engineer on an end-to-end redesign of 3- and 4-phase voltage stabilizers (circuit, enclosure, PCB, firmware); modular reuse cut production cost by $\sim 70\%$ while keeping backward compatibility.

TEACHING EXPERIENCE

Teaching Assistant, Digital Electronics

Aug 2026 – Present

Department of Electrical Engineering, Shiv Nadar Institution of Eminence

- Leading lab sessions for 60 students and designing three FPGA experiments that teach Verilog through progressively harder RTL design tasks.

Curriculum Designer and Lab Instructor, Electronics & IoT

Jul 2025 – May 2026

Department of Electrical Engineering, Shiv Nadar Institution of Eminence

- Designed labs and assessments for a first-year course of 480+ students, taught 120+ students, and led the build-out of a 20-station electronics research lab.

HONORS, SERVICE & OUTREACH

- Anveshana National Science Fair: selected from 20,000+ applicants nationwide; led STEM workshops for 50+ students and presented a secure-IoT prototype to 300+ attendees 2024–25
- Atal Incubation Centre Scholar, Life Link health platform (INR 100K grant) 2024–25
- Invited peer reviewer, IEEE ICNARI 2026

TECHNICAL SKILLS

- *Hardware*: SystemVerilog, Verilog, Amaranth HDL, UVM, formal verification (SymbiYosys), FPGAs
- *Architecture*: instruction-set simulation, cycle-accurate RTL simulation, SEC/SECDED ECC, NoCs
- *Software & ML*: C++, C, Python, Tcl, PyTorch, LLM fine-tuning (LoRA, SFT, RL), quantization
- *EDA & embedded*: Synopsys RTL-to-GDS, Cadence Xcelium & Virtuoso, Vivado, KiCad, STM32